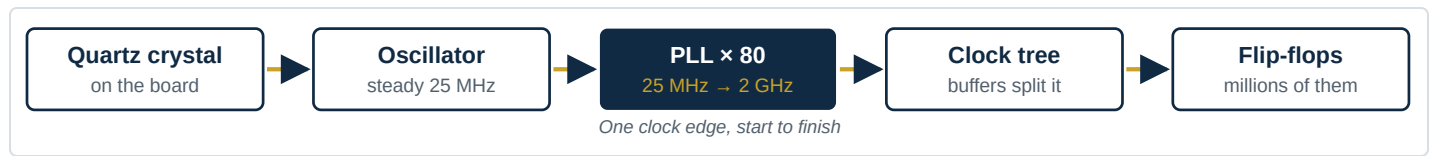


Where does your 2 GHz clock come from?

Every flip-flop in a chip waits for one thing: the clock edge. In this note we follow that one edge from a small quartz crystal on the board, through the PLL, down the clock tree, to the flip-flop. Three steps, nothing more.



1 The quartz crystal gives the first tick

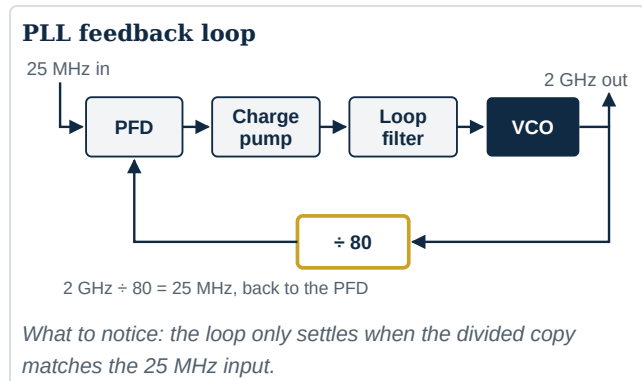
The clock does not start inside the chip. It starts on the board, in a small quartz crystal. Quartz is **piezoelectric**: put a voltage on it and it bends a little, bend it and it gives a voltage back.

Cut to the right size, it vibrates at one fixed frequency and stays very accurate, within a few parts per million. Put an amplifier around it and it keeps vibrating on its own. That is the **crystal oscillator**. Typical outputs are **19.2, 24 or 25 MHz**.

WHY THIS MATTERS

A crystal is accurate but slow. A CPU needs GHz. So we keep the crystal for accuracy and let the PLL do the multiplying.

2 The PLL multiplies it to 2 GHz



The **VCO** makes the fast clock. A copy of it goes through a **divider** that slows it down by N. The **PFD** compares that slowed copy with the 25 MHz input.

If the copy is late, the VCO speeds up. If it is early, the VCO slows down. The **charge pump** and **loop filter** turn this "faster or slower" decision into a smooth control voltage. When both edges line up every cycle, the PLL is **locked**.

$$F_{\text{out}} = F_{\text{ref}} \times N$$

$$25 \text{ MHz} \times 80 = 2,000 \text{ MHz} = 2 \text{ GHz}$$

Some PLLs also divide the input first by M, then $F_{\text{out}} = F_{\text{ref}} \times N / M$.

Word	What it means in plain terms
Lock time	How long the PLL takes to settle after power-up or after you change N.
Jitter	The edge does not land at exactly the same time every cycle. It wobbles a little.
Loop bandwidth	How fast the loop reacts. Faster means quicker lock but more noise from the input gets through.



3 The clock tree carries it to every flip-flop

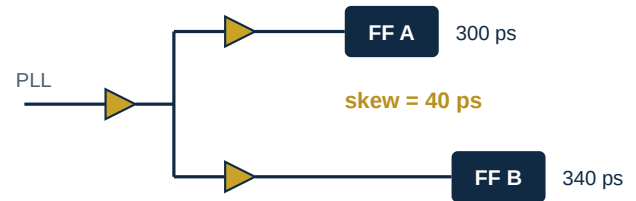
Now one 2 GHz signal has to reach millions of flip-flops. A single wire cannot drive that load, so **CTS** (clock tree synthesis) builds a tree of buffers that splits the clock again and again until every flop gets it.

The tree is never perfect. Some flops sit closer to the source and some farther, so the same edge reaches them at slightly different times. The time from source to a flop is **insertion delay** (also called latency). The difference between two flops is **skew**.

COMMON BEGINNER MISTAKE

Saying skew is always bad. If the capture flop gets the edge later (positive skew), setup gets extra time. The price is paid in hold.

Same edge, two arrival times



What to notice: FF B has a longer path, so the edge reaches it 40 ps later. Example numbers only.

4 Five interview questions, answered the way I would

Q1 Why use a PLL and not a 2 GHz crystal?	Practical crystals run at tens of MHz. The PLL builds GHz inside the chip from a cheap, accurate reference, and you can change N to change the frequency.
Q2 What happens if the PLL loses lock?	The output frequency drifts, the lock-detect signal goes low, and the design keeps logic in reset or gates the clock until the PLL locks again. Until then, timing is not guaranteed.
Q3 Jitter and skew, what is the difference?	Jitter is about time: the same clock edge moves a little from cycle to cycle. Skew is about place: one edge reaches two flops at different times. Both eat into your timing margin.
Q4 Why is the ÷N inside the feedback loop?	The loop keeps adjusting until the divided output equals the reference. So the output has to be N times the reference. Change N and you change the clock.
Q5 Does skew help setup or hold?	Positive skew (capture clock later) helps setup and hurts hold. Negative skew does the opposite. Hold is checked on the same edge, so slowing the clock does not fix a hold violation.

Remember it in three lines

1. The **crystal** gives an accurate but slow tick, around 25 MHz.
2. The **PLL** multiplies it: $F_{\text{out}} = F_{\text{ref}} \times N$, so $25 \text{ MHz} \times 80 = 2 \text{ GHz}$.
3. The **clock tree** delivers it to every flop, and the small arrival differences are **skew**.

TRY THIS

Your reference is 24 MHz and you need a 1.2 GHz clock. What N do you set? (Answer: $1200 / 24 = 50$)

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